10647061

1FW cofc

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re U.S. Patent No. **6,830,964 B1**)
MEARS ET AL.)
)
Issued: **DECEMBER 14, 2004**)
)
For: **METHOD FOR MAKING SEMICONDUCTOR**)
DEVICE INCLUDING BAND-)
ENGINEERED SUPERLATTICE)
)

REQUEST FOR CERTIFICATE OF CORRECTION OF APPLICANT'S MISTAKE UNDER RULE 1.323

Commissioner For Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

In accordance with the provisions of Rule 1.323 of the Rules of Practice, the Patent Office is respectfully requested to correct matters in the above-identified patent in accordance with the Certificate of Correction Form PTO-1050 attached hereto.

The Patent Office is requested to issue a Certificate of Correction on the above-referenced Patent Document, and to place such a Certificate of Correction in the file, so that such will appear on any copies of the patent which are ordered in the future.

The corrections being made are of consequence to provide the proper recitation on the cover page, in the drawings and specification. Several of the mistakes occurred in good faith and are not the fault of the Patent and Trademark Office. However, two printing errors of the Patent Office are also being corrected. No new matter is added by these corrections.

In re Patent of
MEARS ET AL.
Patent No. **6,830,964 B1**
Issued: **DECEMBER 14, 2004**
_____/

Authorization is given to charge the requisite fee as set forth in 37 CFR § 1.20(a) in the amount of $100.00 to the credit card listed on the attached credit card payment form PTO-2038. The Commissioner is authorized to charge or credit any discrepancies in fee amounts to Deposit Account 01-0484.

Respectfully submitted,

CHRISTOPHER F. REGAN
Reg. No. 34,906
Allen, Dyer, Doppelt, Milbrath
& Gilchrist, P.A.
255 S. Orange Ave., Suite 1401
P. O. Box 3791
Orlando, Florida 32802
(407) 841-2330

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: COMMISSIONER FOR PATENTS, P.O. BOX 1450, ALEXANDRIA, VA 22313-1450, on this 15th day of April, 2005.

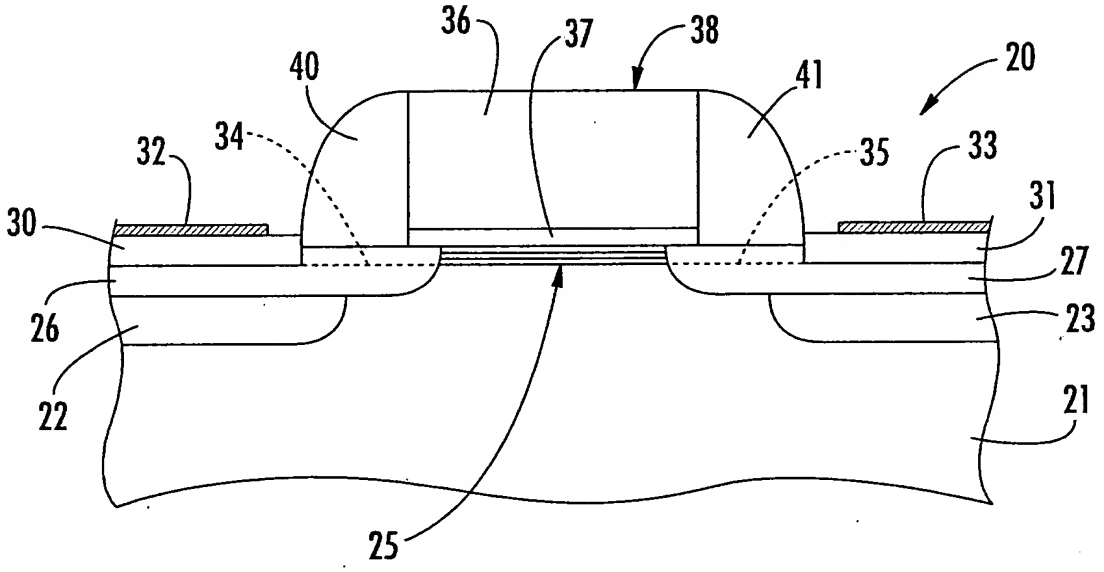
UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO.	:	6,830,964 B1
DATED	:	December 14, 2004
INVENTOR(S)	:	Mears et al.

It is certified that error appears in the above-identified patent and that said Letters Patent are hereby corrected as shown below

Cover Page, Drawing	Delete: FIG. 1 Insert: New FIG. 1



MAILING ADDRESS OF SENDER:
Christopher F. Regan
Allen, Dyer, Doppelt, Milbrath & Gilchrist, P.A.
255 S. Orange Avenue - Suite 1401
P.O. Box 3791
Orlando, FL 32802-3791
PHONE : (407) 841-2330

PATENT NO. 6,830,964 B1

UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO.	:	6,830,964 B1
DATED	:	December 14, 2004
INVENTOR(S)	:	Mears et al.

It is certified that error appears in the above-identified patent and that said Letters Patent are hereby corrected as shown below

In the Drawings Delete: FIG. 1
Insert: New FIG. 1

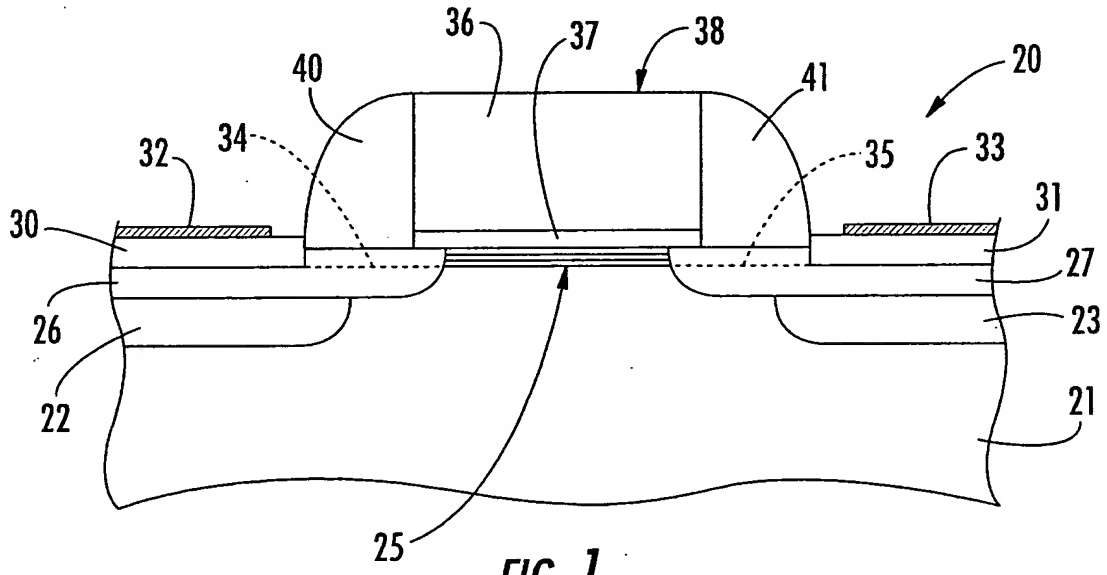


FIG. 1

MAILING ADDRESS OF SENDER:
Christopher F. Regan
Allen, Dyer, Doppelt, Milbrath & Gilchrist, P.A.
255 S. Orange Avenue - Suite 1401
P.O. Box 3791
Orlando, FL 32802-3791
PHONE : (407) 841-2330

PATENT NO. 6,830,964 B1

UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO.	:	6,830,964 B1
DATED	:	December 14, 2004
INVENTOR(S)	:	Mears et al.

It is certified that error appears in the above-identified patent and that said Letters Patent are hereby corrected as shown below

Column 1, Line 44
Delete: "on a binary"
Insert: --on binary--

Column 2, Line 2
Delete: "in a silicon"
Insert: --in silicon--

Column 2, Line 3
Delete: "electromuminescence"
Insert: --electroluminescence--

Column 2, Line 62
Delete: "superlattice and has"
Insert: --superlattice has--

Column 3, Line 49
Delete: "Si/o"
Insert: --Si/O--

Column 4, Line 32
Delete:

$$\mathbf{M}^{-1}_{k,ij}(E_F,T)=\frac{-\sum_{E<E_F}\int_{B.Z.}\left(\nabla_{\mathbf{k}}E(\mathbf{k},n)\right)_i\left(\nabla_{\mathbf{k}}E(\mathbf{k},n)\right)_j\frac{\partial f(E(\mathbf{k},n),E_F,T)}{\partial E}d^3\mathbf{k}}{\sum_{E<E_F}\int_{B.Z.}(1-f(E(\mathbf{k},n),E_F,T))d^3\mathbf{k}}$$

Insert:

$$\mathbf{M}^{-1}_{h,ij}(E_F,T)=\frac{-\sum_{E<E_F}\int_{B.Z.}\left(\nabla_{\mathbf{k}}E(\mathbf{k},n)\right)_i\left(\nabla_{\mathbf{k}}E(\mathbf{k},n)\right)_j\frac{\partial f(E(\mathbf{k},n),E_F,T)}{\partial E}d^3\mathbf{k}}{\sum_{E<E_F}\int_{B.Z.}(1-f(E(\mathbf{k},n),E_F,T))d^3\mathbf{k}}$$

MAILING ADDRESS OF SENDER:
Christopher F. Regan
Allen, Dyer, Doppelt, Milbrath & Gilchrist, P.A.
255 S. Orange Avenue - Suite 1401
P.O. Box 3791
Orlando, FL 32802-3791
PHONE : (407) 841-2330

PATENT NO. 6,830,964 B1

UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO.	:	6,830,964 B1
DATED	:	December 14, 2004
INVENTOR(S)	:	Mears et al.

It is certified that error appears in the above-identified patent and that said Letters Patent are hereby corrected as shown below

Column 5, Line 13	Delete: "gate 35" Insert: --gate 38--
Column 5, Line 61	Delete: "gate 35" Insert: --gate 38--
Column 7, Line 63	Delete: "from the both" Insert: --from both--
Column 9, Lines 44-46	Delete: "In other processes and devices the structures of the present invention may be formed on a portion of a wafer or across substantially all of a wafer."
Column 9, Line 59	Delete: "also formed" Insert: --also be formed--

MAILING ADDRESS OF SENDER:
Christopher F. Regan
Allen, Dyer, Doppelt, Milbrath & Gilchrist, P.A.
255 S. Orange Avenue - Suite 1401
P.O. Box 3791
Orlando, FL 32802-3791
PHONE : (407) 841-2330

PATENT NO. 6,830,964 B1